# KAF- 0401LE

## 768 (H) x 512 (V) Pixel

## Enhanced Response
## Full-Frame CCD Image Sensor
## With Anti-Blooming Protection

## Performance Specification

**Eastman Kodak Company**

**Microelectronics Technology Division**

**Rochester, New York 14650-2010**

**Revision B**
**June 7, 1999**

## TABLE OF CONTENTS

1.1 Features....3
1.2 Description....3
1.3 Image Acquisition....4
1.4 Charge Transport....4
1.5 Output Structure....4
1.6 Dark Reference Pixels....4
1.7 Dummy Pixels....4

2.1 Package Configuration....5
2.2 Pin Description....6

3.1 Absolute Maximum Ratings....7
3.2 DC Operating Conditions....8
3.3 AC Operating Conditions....9
3.4 AC Timing Conditions....9

4.1 Performance Specifications....11
4.2 Typical Performance Characteristics....12
4.3 Defect Classification....13

5.1 Quality Assurance and Reliability....14
5.2 Ordering Information....14

## APPENDICES

Appendix 1 - Part Number Availability....15

## FIGURES

Figure 1 Functional Block Diagram....3
Figure 2 Packaging Diagram....5
Figure 3 Packaging Pin Designations....6
Figure 4 Recommended Output Structure Load Diagram....8
Figure 5 Timing Diagrams....10

Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 1.1 Features

**393K Pixel Area CCD**
**768H x 512V (9 mm) Pixels**
**Transparent Gate True Two Phase Technology (Enhanced Spectral Response)**
**6.91 mm H x 4.6 mm V Photosensitive Area**
**2-Phase Register Clocking**
**70% Fill Factor**
**Antiblooming Protection**
**Low Dark Current ( <7pA/cm$^2$ @ 25$^{o}$C)**

## 1.2 Description

The KAF-0401LE is a high performance monochrome area CCD (charge-coupled device) image sensor with 768H x 512V photo-active pixels designed for a wide range of image sensing applications in the 0.4nm to 1.0nm wavelength band. Typical applications include military, scientific, and industrial imaging. A 67 dB dynamic range is possible operating at room temperature.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor and reduces the dark current without compromising charge capacity. The transparent gate results in spectral response increased ten times at 400nm, compared to a front side illuminated standard poly silicon gate technology. The sensitivity is increased 50% over the rest of the visible wavelengths.

Total chip size is 8. mm x 5.5mm and is housed in a 24-pin, 0.805” wide DIL ceramic package with 0.1” pin spacing.

The sensor consists of 784 parallel (vertical) CCD shift registers each 520 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The elements of these registers are arranged into a 768 x 512 photosensitive array surrounded by a light shielded dark reference of 16 columns and 8 rows. The parallel (vertical) CCD registers transfer the image one line at a time into a single 796 element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo generated charge to a voltage for each pixel.

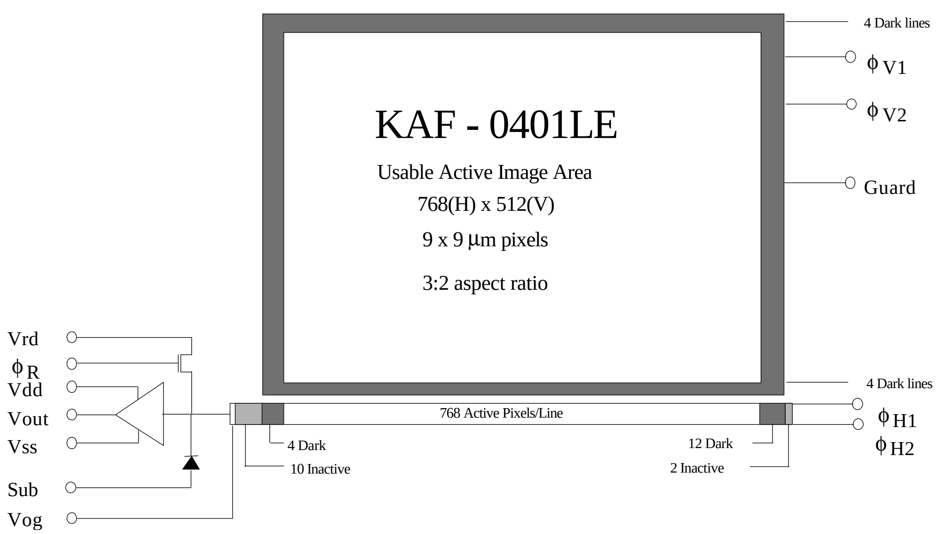



Figure 1. - Functional Block Diagram

## 1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon-induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will spill into the lateral overflow drain (LOD) and drain off chip, thus isolating adjacent pixels from the excess signal. This is termed anti-blooming protection. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level.
See Figure 5. - Timing Diagrams.

The antiblooming capability is provided by a lateral overflow drain structure. This type of anti-blooming design consumes thirty percent of the pixel area and reduces the saturation signal and quantum efficiency proportionately. However, it maintains the broad spectral response from 400 to 1000nm and good linear response up to saturation.

## 1.4 Charge Transport

Referring again to Figure 5 - Timing Diagrams, the integrated charge from each photogate is transported to the output using a two step process. Each line (row) of charge is first transported from the vertical CCDs to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling
edge of ϕH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier

## 1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on FD.
Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and FD is reset to the potential applied by VRD. More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device - see Figure 4.

## 1.6 Dark Reference Pixels

Surrounding the peripheral of the device is a border of light shielded pixels. This includes 4 leading and 12 trailing pixels on every line excluding dummy pixels. There are also 4 full dark lines at the start of every frame and 4 full dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel, or the outer bounds of the chip (including the first two lines out), can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

## 1.7 Dummy Pixels

Within the horizontal shift register are 10 leading and 2 trailing additional shift phases which are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions.

## 2.1 Package Configuration

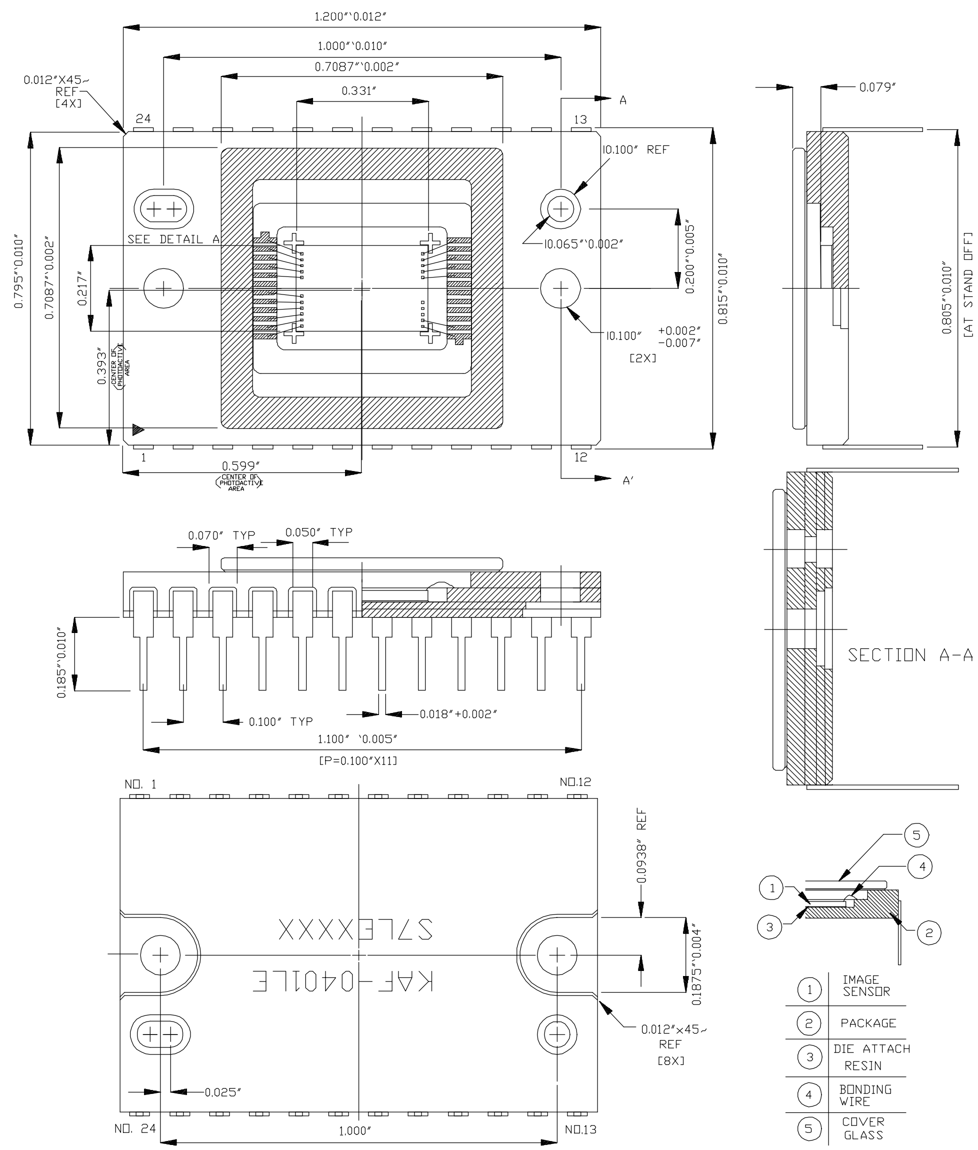


Figure 2 - Package Drawing

## 2.2 Pin Description

| Pin | Symbol | Description | Pin | Symbol | Description |
|---|---|---|---|---|---|
| 1 | VOG | Output Gate | 9, 10, 11, 12 | N/C | No connection (open pin) |
| 2 | VOUT | Video Output | 13 | N/C | No connection (open pin) |
| 3 | VDD | Amplifier Supply | 14 | VSUB | Substrate (Ground) |
| 4 | VRD | Reset Drain | 15, 16, 21, 22 | ϕV1 | Vertical CCD Clock - Phase 1 |
| 5 | ϕR | Reset Clock | 17, 18, 19, 20 | ϕV2 | Vertical CCD Clock - Phase 2 |
| 6 | VSS | Amplifier Supply Return | 23 | Guard | Guard Ring |
| 7 | ϕH1 | Horizontal CCD Clock - Phase 1 | 24 | N/C | No Connection (open pin) |
| 8 | ϕH2 | Horizontal CCD Clock - Phase 2 | | | |

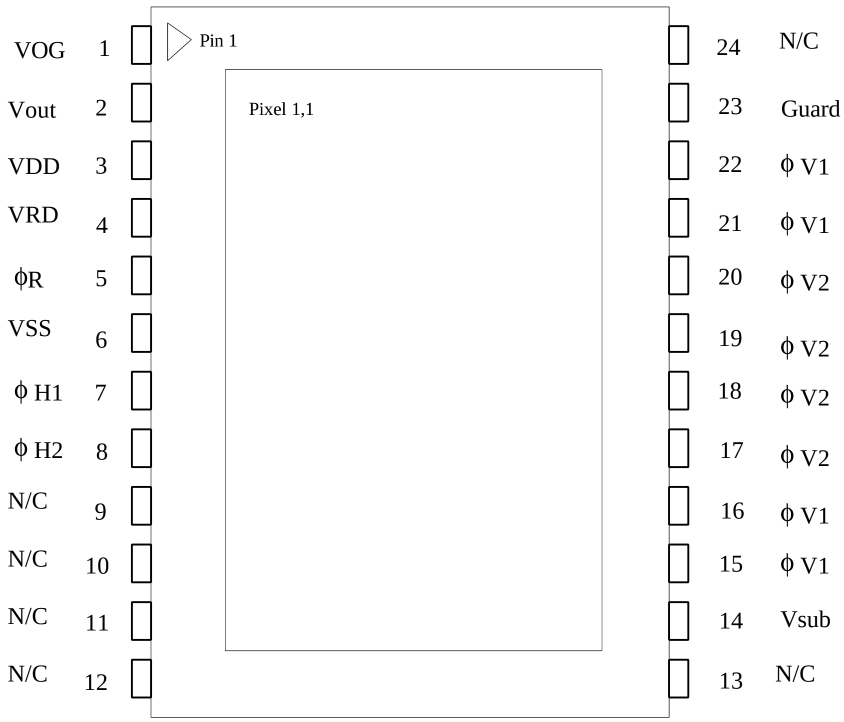



Figure 3 - Packaging Pin Designations

Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 3.1 Absolute Maximum Ratings

| Description | Symbol | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| Diode Pin Voltages | Vdiode | 0 | 20 | V | 1, 2 |
| Gate Pin Voltages - Type 1 | Vgate1 | -16 | 16 | V | 1, 3 |
| Gate Pin Voltages - Type 2 | Vgate2 | 0 | 16 | V | 1, 4 |
| Inter-Gate Voltages | Vg-g | | 16 | V | 5 |
| Output Bias Current | Iout | | -10 | mA | 6 |
| Output Load Capacitance | Cload | | 15 | pF | 6 |
| Storage Temperature | T | | 100 | $^{o}$C | |
| Humidity | RH | 5 | 90 | % | 7 |

**Notes:**
1. Referenced to pin VSUB.
2. Includes pins: VRD, VDD, VSS, VOUT.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2.
4. Includes pins: ϕR, VOG.
5. Voltage difference between overlapping gates. Includes: ϕV1 to ϕV2, ϕH1 to ϕH2, ϕV2 to ϕH1, ϕH2 to VOG.
6. Avoid shorting output pins to ground or any low impedance source during operation.
7. T=25°C. Excessive humidity will degrade MTTF.

| | |
|---|---|
| **CAUTION:** | **This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 1 devices.** |

Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 3.2 DC Operating Conditions

| Description | Symbol | Min. | Nom. | Max. | Units | Max DC Current (mA) | Notes |
|---|---|---|---|---|---|---|---|
| Reset Drain | VRD | 10.5 | 11 | 11.5 | V | 0.01 | |
| Output Amplifier Return | VSS | 1.5 | 2.0 | 2.5 | V | -0.5 | |
| Output Amplifier Supply | VDD | 14.5 | 15 | 15.5 | V | Iout | |
| Substrate | VSUB | 0 | 0 | 0 | V | 0.01 | |
| Output Gate | VOG | 3.75 | 4 | 5 | V | 0.01 | |
| Guard Ring | Guard | 8.0 | 9.0 | 12.0 | V | 0.01 | |
| Video Output Current | Iout | | -5 | -10 | mA | - | 1 |

**Notes:**
1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

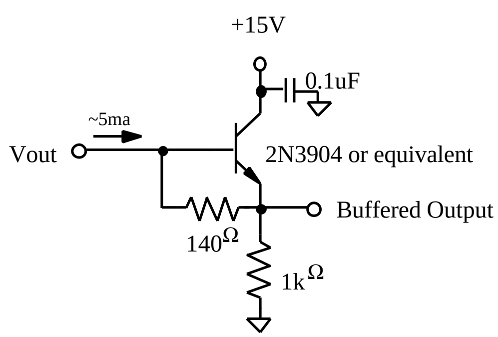



Figure 4 - Recommended Output Structure Load Diagram

## 3.3 AC Operating Condition

| Description | Symbol | Level | Min. | Nom. | Max. | Units | Effective Capacitance |
|---|---|---|---|---|---|---|---|
| Vertical CCD Clock - Phase 1 | $\phi V1$ | Low<br>High | -10.5<br>0 | -10.0<br>0.5 | -9.5<br>1.0 | V<br>V | 6 nF<br>(all øV1 pins) |
| Vertical CCD Clock - Phase 2 | $\phi V2$ | Low<br>High | -10.5<br>0 | -10.0<br>0.5 | -9.5<br>1.0 | V<br>V | 6 nF<br>(all øV2 pins) |
| Horizontal CCD Clock - Phase 1 | $\phi H1$ | Low<br>High | -5.0<br>5.0 | -4.0<br>6.0 | -3.5<br>6.5 | V<br>V | 50 pF |
| Horizontal CCD Clock - Phase 2 | $\phi H2$ | Low<br>High | -5.0<br>5.0 | -4.0<br>6.0 | -3.5<br>6.5 | V<br>V | 50 pF |
| Reset Clock | $\phi R$ | Low<br>High | -4.0<br>3.5 | -3.0<br>4.0 | -2.0<br>5.0 | V<br>V | 5pF |

**Notes:**
1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.

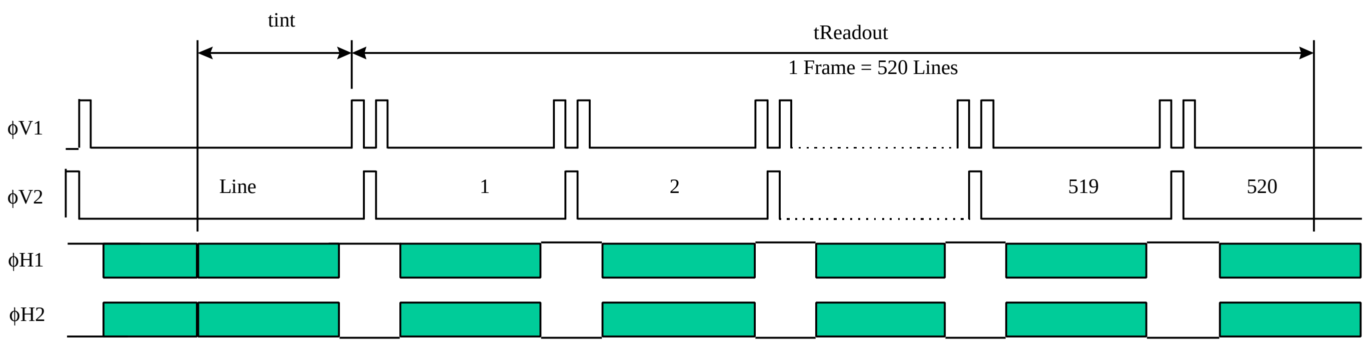
## 3.4 AC Timing Conditions

| Description | Symbol | Min. | Nom. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| $\phi$H1, $\phi$H2 Clock Frequency | $f_H$ | | 10 | 15 | MHz | 1, 2, 3 |
| $\phi$V1, $\phi$V2 Clock Frequency | $f_V$ | | 100 | 125 | kHz | 1, 2, 3 |
| Pixel Period (1 Count) | $t_e$ | 67 | 100 | | ns | |
| $\phi$H1, $\phi$H2 Setup Time | $t_{\phi HS}$ | 0.5 | 1 | | us | |
| $\phi$V1, $\phi$V2 Clock Pulse Width | $t_{\phi V}$ | 4 | 5 | | us | 2 |
| Reset Clock Pulse Width | $t_{\phi R}$ | 10 | 20 | | ns | 4 |
| Readout Time | $t_{readout}$ | 34 | 50 | | ms | 5 |
| Integration Time | $t_{int}$ | | | | | 6 |
| Line Time | $t_{line}$ | 65.8 | 95.6 | | us | 7 |

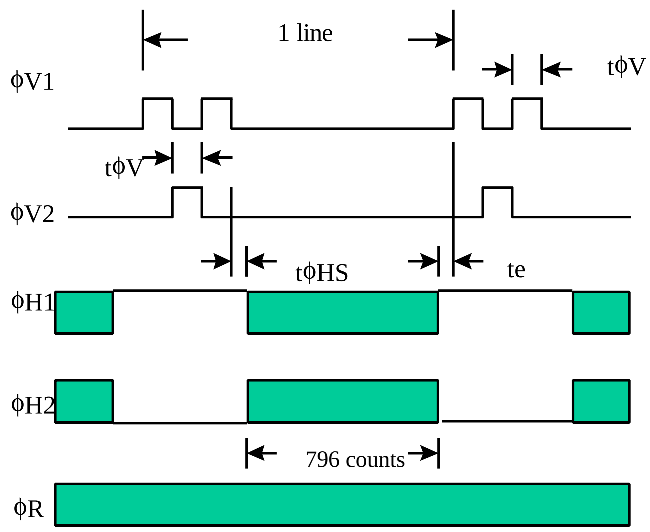
**Notes:**
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. fR should be clocked continuously.
5. $t_{readout} = ( 1032 * t_{line} )$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = ( 3 * t_{\phi V} ) + t_{\phi HS} + ( 1564 * t_e ) + t_e$

Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

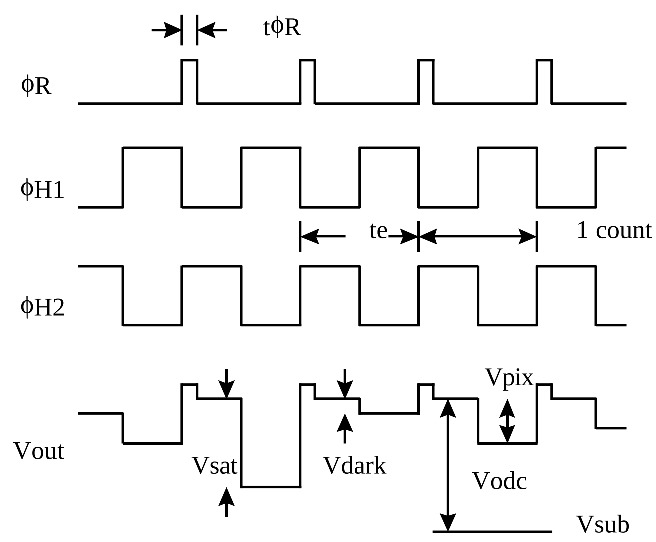
## Frame Timing



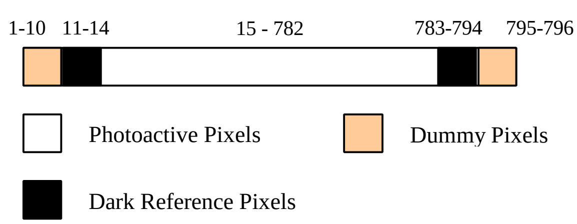

## Line Timing Detail




## Pixel Timing Detail




### Line Content




| | |
|---|---|
| Vsat | Saturated pixel video output signal |
| Vdark | Video output signal in no light situation, not zero due to Jdark |
| Vpix | Pixel video output signal level, more electrons =more negative* |
| Vodc | Video level offset with respect to vsub |
| Vsub | Analog Ground |

* See Image Aquisition section (page 4)

Figure 5 - Timing Diagrams

## 4.1 Performance Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

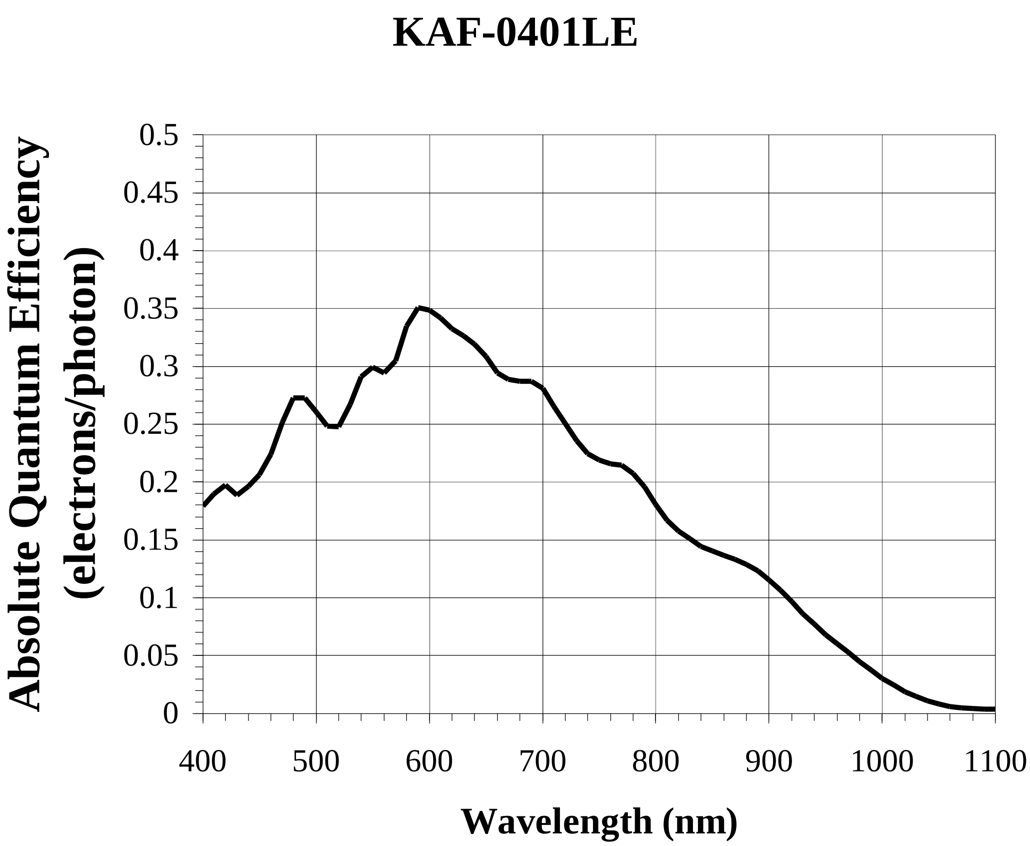
| Description | Symbol | Min. | Nom. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| Saturation Signal<br>Vertical CCD capacity<br>Horizontal CCD capacity<br>Output Node capacity | Nsat | 45000<br>170000<br>190000 | 50000<br>200000<br>220000 | 65000<br>240000<br>240000 | electrons / pixel | <br><br><br>1 |
| Red Quantum Efficiency (λ=650nm)<br>Green Quantum Efficiency (λ=550nm)<br>Blue Quantum Efficiency (λ=450nm)<br>Blue Quantum Efficiency (λ=400nm) | Rr<br>Rg<br>Rb<br>Rb 400 | | 42<br>35<br>20<br>16 | | %<br>%<br>%<br>% | |
| Photoresponse Non-Linearity | PRNL | | 1 | 2 | % | 2 |
| Photoresponse Non-Uniformity | PRNU | | 1 | 3 | % | 3 |
| Dark Signal | Jdark | | 15<br>2.1 | 35<br>7 | electrons / pixel / sec<br>$pA/cm^2$ | 4 |
| Dark Signal Doubling Temperature | | 5 | 6.3 | 7.5 | °C | |
| Dark Signal Non-Uniformity | DSNU | | 25 | 50 | electrons / pixel / sec | 5 |
| Dynamic Range | DR | 67 | 70 | | dB | 6 |
| Charge Transfer Efficiency | CTE | 0.99997 | 0.99999 | | | |
| Output Amplifier DC Offset | Vodc | 9.5 | 10.5 | 11.5 | V | 7 |
| Output Amplifier Bandwidth | $f_{-3dB}$ | | 45 | | Mhz | 8 |
| Output Amplifier Sensitivity | Vout/Ne~ | 9 | 10 | 11 | uV/e~ | |
| Output Amplifier output Impedance | Zout | 175 | 200 | 250 | Ohms | |
| Noise Floor | ne~ | | 15 | 20 | electrons | 9 |
| Antiblooming Protection | Vab | 128 | | | Saturation exposure | 10 |

**Notes:**

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs.
   Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25 °C..
5. Average dark signal of any of 6 x 4 blocks within the sensor. (each block is 128 x 128 pixels)
6. 20log ( Nsat / ne~) at nominal operating frequency and 25°C.
7. Video level offset with respect to ground
8. Last output amplifier stage only. Assumes 10pF off-chip load..
9. Output noise at 25 °C , nominal operating frequency, and tint = 0.
10. Number of times above the Vsat illumination level required to cause 50% distortion in a test pattern consisting of a bright circular region approximately 1/10 the size of the image sensor. In most systems a 128x optical overload will cause flare from reflections that mask the performance of the image sensor.

## 4.2 Typical Performance Characteristics

**Spectral Response**

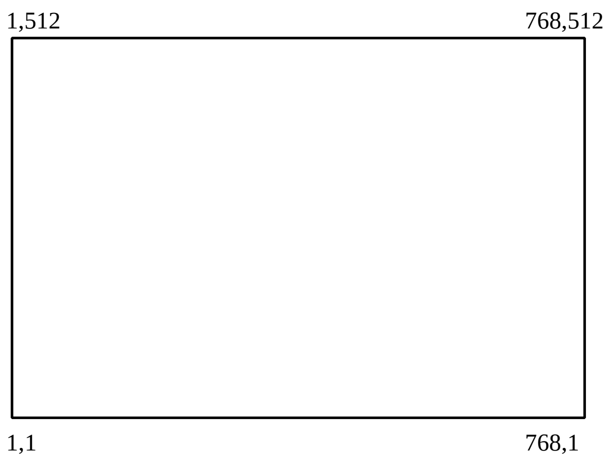



Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com

## 4.3 Defect Classification

Defect tests performed at T=25°C

| Class | Point Defects Total | Cluster Defects Total | Column Defects Total |
|---|---|---|---|
| C0 | 0 | 0 | 0 |
| C1 | ≤5 | 0 | 0 |
| C2 | ≤10 | ≤4 | 0 |




| | |
|---|---|
| Point Defect | DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR<br>BRIGHT: A Pixel with dark current > 3000 e/pixel/sec at 25C. |
| Cluster Defect | A grouping of not more than 5 adjacent point defects |
| Column Defect | A grouping of >5 contiguous point defects along a single column, OR<br>A column containing a pixel with dark current > 6,000e/pixel/sec, OR<br>A column that does not meet the minimum vertical CCD charge capacity, OR<br>A column which loses more than 250 e under 2Ke illumination. |
| Neighboring pixels | The surrounding 128 x 128 pixels or ±64 columns/rows. |
| Defect Separation | Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects). |
| Defect Region Exclusion | Defect region excludes the outer two (2) rows and columns at each side/end of the sensor. |

## 5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in a static-safe container and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Microelectronics Technology Division and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number of traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

## 5.2 Ordering Information

See Appendix 1 for available part numbers

Address all inquiries and purchase orders to:

Microelectronics Technology Division
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (716) 722-4385
Fax: (716) 477-4947
E-mail: CCD@kodak.com

Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

**WARNING: LIFE SUPPORT APPLICATIONS POLICY**

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

# Appendix

## Appendix 1 - Part Number Availability

Note: This appendix may be updated independently of the performance specification. Contact Eastman Kodak for the latest revision

| Device Name | Available Part Numbers | Features |
|---|---|---|
| KAF-0401LE | 2H4503 | Clear Sealed Glass, Class 2 |
| KAF-0401LE | 2H4504 | Clear Sealed Glass, Engineering Grade |
| KAF-0401LE | 2H4505 | Clear Sealed Glass, Mechanical Grade |
| KAF-0401LE | 2H4499 | Clear Taped Glass, Engineering Grade |
| KAF-0401LE | 2H4500 | Clear Taped Glass, Mechanical Grade |

Eastman Kodak Company - Microelectronics Technology Division - Rochester, NY 14650-2010
Phone (716) 722-4385 Fax (716) 477-4947
Web: www.kodak.com/go/ccd E-mail: ccd@kodak.com